MULTIPROCESSOR CACHE COHERENCE SYSTEM AND METHOD IN WHICH PROCESSOR NODES AND INPUT/OUTPUT NODES ARE EQUAL PARTICIPANTS

ABSTRACT OF THE DISCLOSURE

A computer system has a plurality of processor nodes and a plurality of input/output nodes. Each processor node includes a multiplicity of processor cores, an interface to a local memory system and a protocol engine implementing a predefined cache coherence protocol. Each processor core has an associated memory cache for caching memory lines of information. Each input/output node includes no processor cores, an input/output interface for interfacing to an input/output bus or input/output device, a memory cache for caching memory lines of information and an interface to a local memory subsystem. The local memory subsystem of each processor node and input/output node stores a multiplicity of memory lines of information. The protocol engine of each processor node and input/output node implements the same predefined cache coherence protocol.